A Portable 3D FFT Package for Distributed Memory Parallel Architectures

Iong Q. Ding, Robert 1). Ferraro, and Donald B. Gennery
Jet Propulsion Laboratory, Mail Code 16!3-315
California Institute of Technology
Pasadena, CA 91109

Abstract.

On a distributed memory massively parallel supercomputer, wc are implementing parallel algorithms for 3D FFTs, which are carried out as a series of (local) sequential 1 D FFTs through a series of data transposes such that all data with coordinates along the dimension in which the 1D FFT is performed are present in this processor. In an 1 D data distribution, each processor contains a number of complete x-y planes of the 3D data. Fully optimized and assembly coded sequential FFTs, such as BLAS routines, arc used in the algorithm. After the FFT's in the x and y dimensions are carried out, wc do a global data transpose to a data distribution in which each processor now contains the complete x-z planes so that FFT's along the z-dimension can be carried out. 31) FFTs with 2D and 3D data distributions are similarly carried out.

Wc designed a local permutation algorithm which reshuffles data locally to allow the global data transpose be carried out in place, reducing the memory requirement of the algorithm from the usual two copies of the input data to just onc copy of the input data: the 3D FFT is done in place. No extra memory is needed except a small buffer for communications.

The package has been implemented for 1D and 2D data distributions. For the 1D data decomposition, a 3D forward and inverse FFT of 256x256x256 real data on a 16-node Paragon takes 6.1 second. (This should be compared with 2.7sec on a CRAY C-90 for a single forward FFT on complex data of the same size, using the CRAY assembly library routine). In scaling runs with fixed size per processor on Intel Delta up to 128 nodes, total time grows slower than log(P), where P is the total number of processors.

Wc are currently extending the FFT package to 3D data decomposition and to more choices of x,y,z orientations along the processor dimensions.